ELLIOTT 900

Volume 1: FUNCTIONAL SPECIFICATION

Part 3: OPTIONAL UNITS

Section 2: NPL INTERFACE MATCHING UNIT

Contents

IN-TEXT FIGURES

Chapter 1: INTRODUCTION

1. 1 General Description

The NPL Interface Matching Unit enables any equipment which has been designed for the NPL interface, to be used with the 900 computer system. The matching unit is an optional unit of the 900 computer and is built into two shelves (i. e. a shelf of logic and a shelf of plugs and sockets). It may be provided with up to four pairs of NPL digital interface plugs and sockets, together with the necessary logic, for the connection of up to four devices designed to use the NPL interface. (One input highway and one output highway are supplied per NPL device and together comprise one channel).

Instructions from the 900 enable the matching unit to transfer data or control information between the 900 computer and any one of the four NPL devices (see Fig. A).

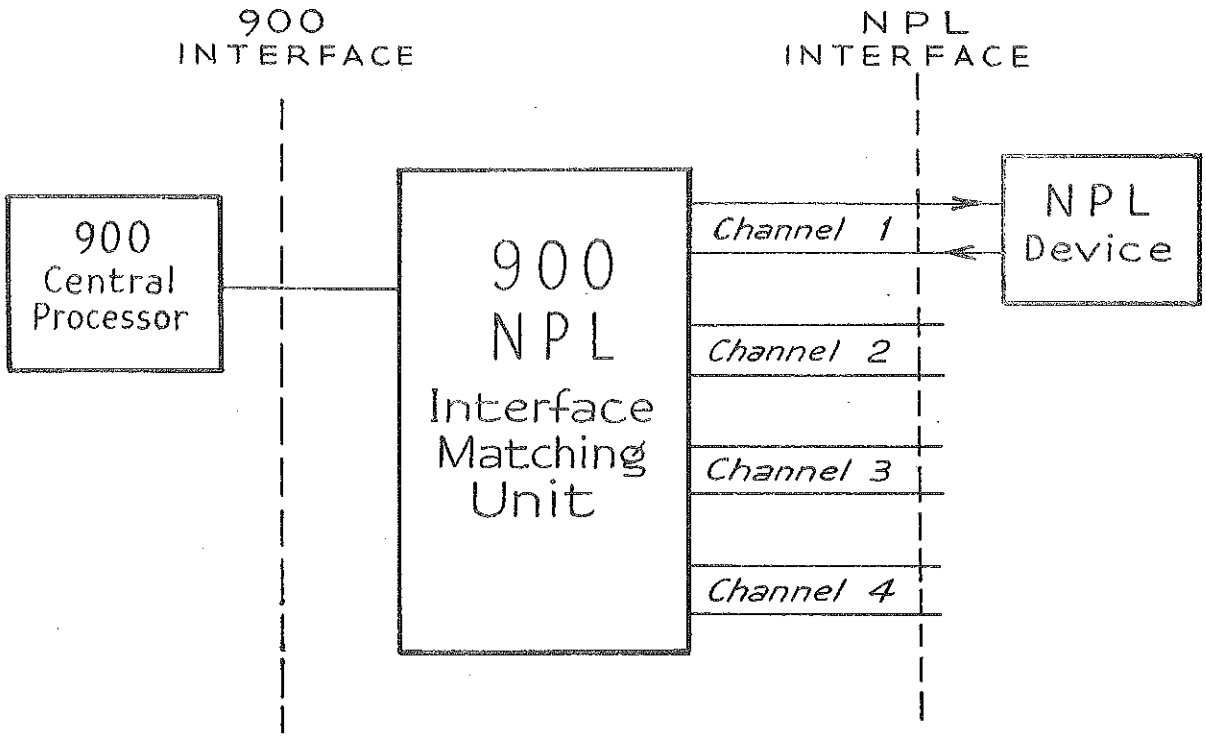

Fig. A Transfer of Data

It should be noted that it is possible to connect an input device and an output device to the same channel.

1.2 Connections to a 900 System

The matching unit is connected to the 900 system via standard 900 peripheral cables.

Chapter 2: TRANSFER OF DATA

2.1 Introduction

Any of the four NPL interface plugs on the matching unit may be connected to the NPL interface socket on the device, thus providing the highway whereby data is input to the central processor from the device. The NPL interface plugs each carry eight pins for the transfer of 8-bit data characters. These pins are lettered from A to H, where A carries the data bit being transferred to the least significant end of the accumulator. In addition, pins J and K carry control signals, pin L is signal earth and pin M is not used.

Similarly, an NPL interface plug on a device may be connected to any NPL interface socket on the matching unit, thus providing the highway whereby data is output from the central processor to the device. The NPL interface sockets carry pins corresponding to those on the interface plugs and, similarly, pin A carries the data bit transferred from the least significant end of the accumulator.

The maximum data transfer rate is 4, 500 characters per second (see Chapter 3).

2.2 Selection of Plug or Socket

The plugs and sockets on the matching unit are numbered from 1 to 4 inclusive. A particular plug or socket for a data transfer is specified by the two least significant bits of the instruction address (see Para. 2. 5).

2.3 Input

Data is transferred from a device to the 900, via the appropriate plug on the matching unit, when the device has data to be read. When data is ready for input, the device makes pin J true and pin K is then made false by the matching unit. When pin J becomes true, an INTERRUPT signal is produced which may be used to cause the computer to jump to an input routine. When the 900 has accepted the data, pin K is made true and the device may remove the data and make pin J false. When fresh data is ready to be read, pin J becomes true and pin K becomes false. (Pin K will remain false for a minimum of 10μs). In this way, successive 8-bit data characters are read in to the processor from a device.

2.4 Output

Data is transferred from the 900 to a device, via the appropriate socket on the matching unit, when the device is ready for the new data. When the device is ready to receive data it makes pin K true. Between transfers pin J is held false by the matching unit. When the 900 obeys an output instruction it places the data word on pins A to H and makes pin J true. (This occurs a minimum of 10μs after pin J is made false). Pin K is made false by the device. When the data is accepted, pin K is made true, ready to receive new data. (The use of an NPL buffer store module, which is able to hold one data character, is recommended in order to avoid the central processor being held-up until pin K becomes true). In this way, successive 8-bit data characters are transferred from the processor to the device.

2.5 Instructions

Any one of four channels can be specified by the two least significant bits of the instruction address. If a non-existent channel is addressed, the matching unit is held-up.

There are two instructions used to transfer data to the computer from the device:

(1) 15 n, Single Character Input

This instruction causes data to be transferred from the device to the eight least significant bits of the accumulator. The remaining 10 bits of the accumulator are cleared. n specifies the particular NPL plug (and hence channel) required.

(2) 14 2048 + n, Block Input

This instruction causes x 8-bit characters to be transferred from the device to store locations y to y+x-1 (where y is the content of the accumulator and x is the content of the Q register). n specifies the particular NPL plug (and hence channel) required. The eight bits are transferred to the eight least significant bits of each word.

There are two instructions used to transfer data from the computer to the device.

(1) 15 4096 + n, Single Character Output

This instruction causes the eight least significant bits from the computer to be transferred to the device. n specifies the particular NPL socket (and hence channel) required.

(2) 14 4096 + n, Block Output

This instruction causes x 8-bit characters to be transferred to the device from store locations y to y+x-1 (where y is the content of the accumulator and x is the content of the Q register). n specifies the particular NPL socket (and hence channel) required. The eight bits transferred are the eight least significant bits of each word.

It should be noted that whilst channel numbers are in the range 1 to 4, the corresponding values of n are in the range 0 to 3. Thus channel 1 is specified by n = 0, channel 2 by n = 1, etc.

2.6 Interrupts

The matching unit will send an INTERRUPT signal to the central processor when a channel becomes ready to input data to the computer. The signal may be on any one of the three INTERRUPT levels and the level can be altered by an engineer.

The INTERRUPT line is held true when a channel is ready to send data to the central processor. The INTERRUPT line is made false again when an appropriate data input transfer is initiated.

It should be noted that a channel can have any of the three INTERRUPT levels connected to it.

2.7 Status Word

The provision of a status word is an optional facility. It provides the programmer with an indication of which channel has interrupted. Bits 5 to 18 of the status word are all '0's; bits 1 to 4 are used to indicate the status of each of the four input channels. The instruction 15 16, Input Status Word, causes the status word to be read from the device to the four least significant bits of the accumulator.

When a channel has a character ready for input, the corresponding bit in the status word is a '1'; it becomes a '0' after the character has been transferred. (Bit 1 of the status word corresponds to channel 1, bit 2 to channel 2, etc). It should be noted that if an NPL channel is not present, the corresponding bit in the status word will be made a '1'. If no NPL device is connected to a channel, the corresponding bit in the status word is made a '0'.

Chapter 3: NOISE REJECTION

Noise rejection facilities are fitted to two lines per interface only (i. e. to pin J on the interface plug and pin K on the interface socket). These circuits cause a 100μs delay in the recognition of positive-going edges and 10μs in the recognition of negative-going edges. Thus, transmission and reception of a character takes approximately 220μs and, hence, the number of characters that may be transmitted (or received) is limited to approximately 4, 500 per second.

Chapter 4: NPL SIGNAL LEVELS

The NPL (source) signal levels are:

Logic '1' (or TRUE)	12V ± 1V
Logic '0' (or FALSE)	0V ± 1V

The NPL (detection) signal levels are:

Logic '1' (or TRUE)	12V ± 3V
Logic '0' (or FALSE)	0V ± 3V

The NPL impedance levels are:

Output Impedance	2.2KΩ nominal
Input Impedance	27KΩ nominal

Chapter 5: PHYSICAL FEATURES AND REQUIREMENTS

5. 1 Introduction

Physical details, environmental conditions and power supplies for the NPL Interface Matching Unit are given in this chapter.

5. 2 Weight and Dimensions

The matching unit, complete with power supplies, occupies half a standard 900 desk. The weight of the matching unit and dimensions of the standard desk are given below:-

Height		Width		Depth		Weight	
cm	in	cm	in	cm	in	kg	lb
94	37	109.2	43	66	26	40	90

5. 3 Environmental Conditions

The NPL Interface Matching Unit has been designed to be used in a normal office environment where the following conditions are assumed to apply:

Temperature	10°C to 30°C	(50°F to 86°F)
Relative Humidity	20% to 95%	without condensation

No specific dust control other than reasonable standards of cleanliness.

Under these conditions external environmental control is not normally required.

5. 4 Power Supplies

The mains power supply for the equipment is

230V ± 10% at 50 c/s ± 2%

The power consumption should not exceed

35VA